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# Solution-processed organic crystals for field-effect transistor arrays with smooth semiconductor/dielectric interface on paper substrates

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ABSTRACT

Large surface roughness is a major obstacle for electronic systems fabricated on paper substrates. Here, a mixture solution of organic semiconductor and polymer dielectric was spin-coated on paper substrate with a patterned wettability. This spin-coating process produced organic crystals and a very smooth semiconductor/dielectric interface with a low trap density in well-confined patterns. Despite the large roughness of the paper substrate, the fabricated transistor arrays exhibited high performance with a field-effect mobility reaching 1.3 $cm^2/V\,s$ and an on/off ratio of $10^8$. The presented results offer a simple fabrication method for the current rapidly developing technology of paper electronics.



## 1. Introduction

In recent years, solution-processed organic field-effect transistors (OFETs) on paper substrates have been the subject of intensive interest because of their applications in low-cost and large-area devices [1–4]. However, the large surface roughness of paper substrates is a major obstacle. This roughness typically causes limited performance by inducing a more disordered molecular structure of semiconductors, and can even determine the functionality of devices. The reported carrier mobility is generally lower than 0.1 $cm^2/V\,s$ [2]. Besides, another important issue is that, on paper substrate, organic materials can exhibit only amorphous or polycrystalline thin films. Thus, even based on thermally evaporated organic materials, the highest reported value of carrier mobility of the devices on paper substrates is ~0.5 $cm^2/V\,s$ [5]. To achieve higher mobility, organic crystals have been considered as promising materials by virtue of their highly ordered molecules [6–10], but have not yet been realized as active materials on paper substrates. The limitation arises from the large surface roughness of paper substrates, and subsequently the lack of specific surface modifications on paper substrates for organic crystal growth. In addition, large surface roughness is one of the most important causes of the low on/off ratio ($<10^4$) obtained from reported devices on paper substrates [1–5]. Moreover, in order to turn organic crystals into a viable semiconductor technology, patterning the organic crystals into well-defined geometric feature is desirable [11–16]. At present, the most common approach for patterning solution-processed organic materials is to modify the surface wettability of the substrates using self-assembled molecules (SAMs) [14–16]. Although this approach has been well applied to $SiO_2$/Si and plastic substrates, the requirements of SAM deposition excludes paper substrates for this application. Consequently, developing a technique for fabricating solution-processed organic crystals with a smooth semiconductor/dielectric interface in well-defined patterns for FET arrays on paper substrates is greatly interesting and favorable for future applications of paper electronics.

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In this work, solution-processed organic crystals for FET arrays on paper substrates are presented (Fig. 1a). The surface wettability of the paper substrate was patterned using a hydrophobic polymer dielectric. A simple spin-coating process under ambient conditions produced organic crystals. The resulting transistor arrays exhibited a field-effect mobility ($\mu_{FET}$) reaching 1.3 $cm^2/V$ s and an on/off ratio of $10^8$. The spin-coating process led to a very smooth crystal/dielectric interface with a low trap density. The presented results confirmed the potential of the proposed method for applications in paper electronics.

## 2. Experimental

The paper substrates used in this work were commercially available photo papers (Fujifilm WP2L10PRO). Considering the high water absorption property of paper, a protective layer that can resist water and chemicals was formed by the vacuum deposition of a parylene layer with a thickness of 3 μm [3]. Fig. 1b shows the device structure. First, the bottom gate electrodes were formed by evaporating 60 nm Au through a shadow mask. Then, CYTOP (80 wt.%) was spin-coated onto the substrates under ambient conditions. The CYTOP layer was naturally dried without any thermal treatment. Afterwards, the substrate was covered with a shadow mask and subjected to $O_2$-plasma treatment (60 W) for 5 min. Fig. 2a shows the microscope images of the patterned CYTOP film after $O_2$-plasma treatment on the Au bottom gate arrays. The size of the patterned region was $0.5 \times 0.2$ $mm^2$ with a depth of 40 nm. The perfluorinated polymer of CYTOP has a highly hydrophobic surface with a contact angle of ~105° (Fig. 2b). After the $O_2$-plasma treatment, the patterned regions became

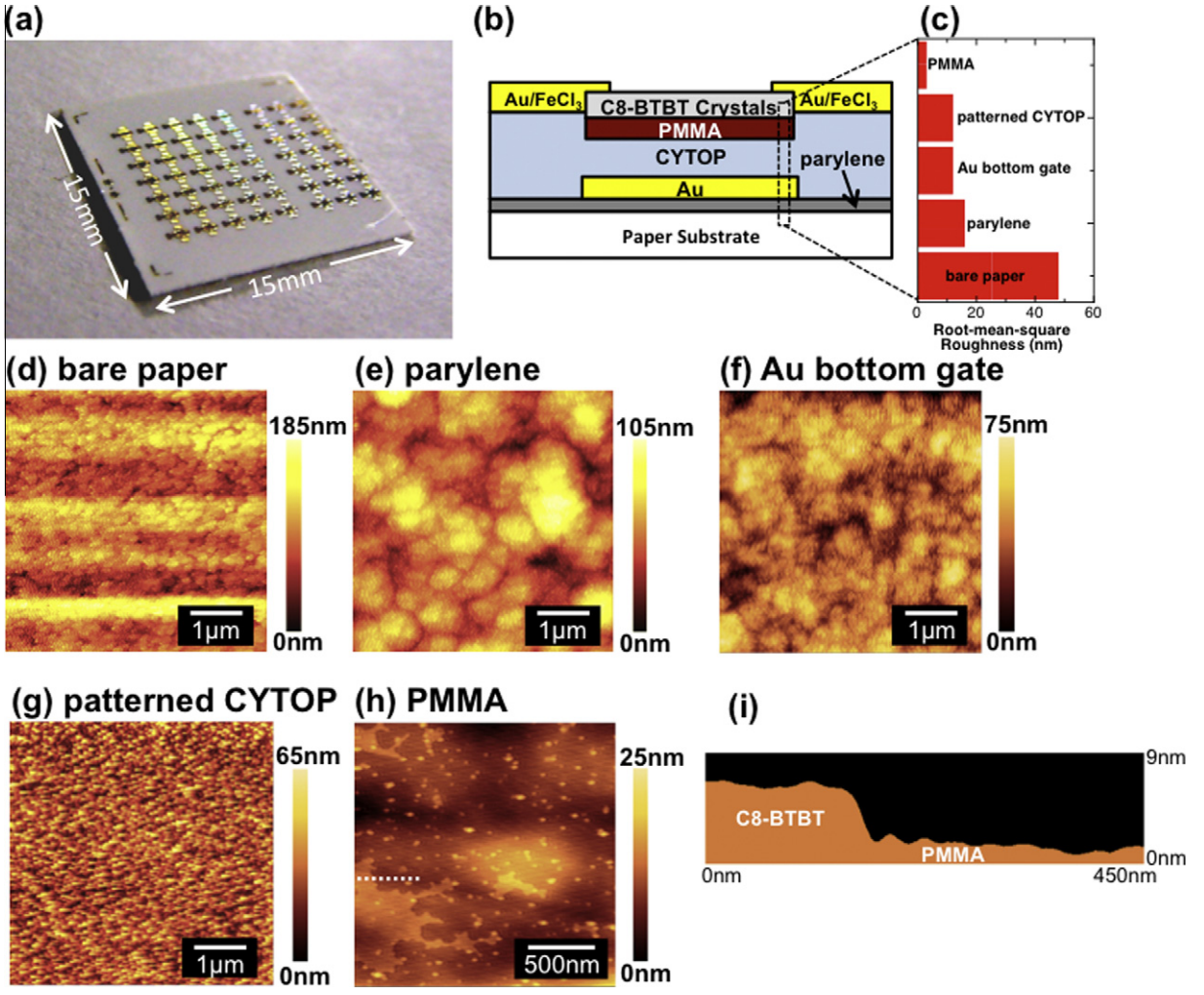


**Fig. 1.** (a) Field-effect transistor (FET) arrays fabricated on paper substrate ($15 \times 15$ $mm^2$) with solution-processed organic crystals confined in patterned regions. (b) Schematic structure of the FETs with dioctylbenzothienobenzothiophene (C8-BTBT) crystals. (c) Root-mean-square (rms) roughness of the different surfaces from the bare paper substrate to the PMMA layer. (d)–(g) Atomic force microscopy (AFM) topographic images of the surfaces of bare paper substrate, parylene, Au bottom gate, and CYTOP at the patterned region, respectively. (h) AFM topographic image of a patterned region after rinsing in cyclohexane. The PMMA surface was exposed and partially covered with C8-BTBT. (i) The AFM profile taken across the broken line over a patch in (h). And indicating that the patches have similar thicknesses, consistent with the length of the C8-BTBT molecule.

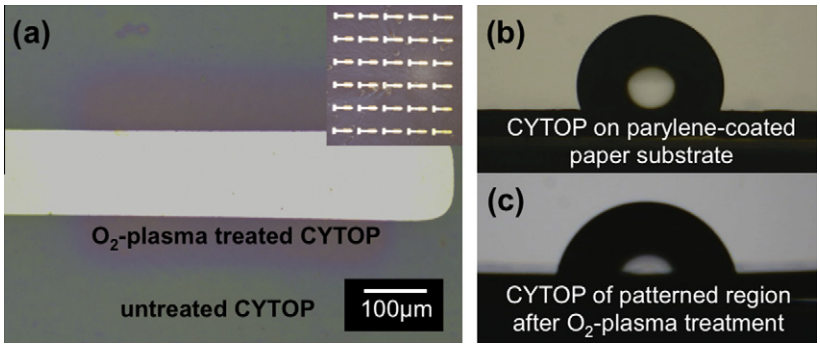


**Fig. 2.** (a) Microscope image of a patterned region by $O_2$-plasma treatment. The inset shows the CYTOP film patterned by the $O_2$-plasma treatment on the Au bottom gate arrays, (b) and (c) images of the water contact angles for an untreated CYTOP surface, and that after 5 min of $O_2$-plasma treatment, respectively.

relatively hydrophilic with a contact angle of ~70° (Fig. 2c). CYTOP also has a low dielectric constant of 2.1 and high dielectric breakdown strength. Therefore, the remaining 500 nm CYTOP in the pattern regions after $O_2$-plasma treatment acted as the bottom-gate dielectric. A naturally dried CYTOP layer has also been applied as a top gate dielectric for OFETs [17]. After patterning the surface wettability, a mixture solution of dioctylbenzothienobenzothiophene (C8-BTBT, 0.4 wt.%) and polymethylmethacrylate (PMMA, 0.1 wt.%) in anisole was spin-coated onto the substrates under ambient conditions (500 rpm for 5 s and 4000 rpm for 200 s). Because of the wettability difference, small droplets were confined within the patterned regions after spin-coating. A double layer structure, with ~10 nm PMMA underneath C8-BTBT, was simultaneously formed during the spin-coating process because of phase separation [18,19]. Finally, $FeCl_3$ and Au were thermally evaporated subsequently through a shadow mask to form the source and drain electrodes. The abovementioned fabrication process resulted in organic crystal FET arrays, and more importantly, in a very smooth semiconductor/dielectric interface on the commercial paper. Device performance of the FET arrays was characterized under vacuum using an Agilent 4156C semiconductor parameter analyzer. Besides, the devices were inevitably exposed to ambient conditions during loading/unloading as well as transfer between one equipment and another.

## 3. Results and discussion

C8-BTBT is a dissolvable semiconducting small molecule that can show good device performance in FETs. It can exhibit a polycrystalline phase or form into rod-like crystals via different deposition techniques and post-deposition treatments [14–18,20,21]. In the presented method, a simple and direct spin-coating process from the mixture solution of C8-BTBT and PMMA led to plate-like C8-BTBT crystals. Figs. 3a and b show the bright-field and cross-polarized microscope images of the C8-BTBT crystals in the channel region, respectively. The grain sizes of crystals were as large as hundreds of micrometers. The crystals showed strong birefringence under cross-polarized light, confirming their crystalline nature. In addition, as seen in Fig. 3c, the crystals changed their colors when the substrate was rotated 45°, indicating that each crystal was assembled with the same crystal orientation. Moreover, Fig. 3d shows typical C8-BTBT crystals, as highlighted by the red dotted square in Fig. 3b. The angle of facets at the crystal front end was ~108°, consistent with the angle between the crystal planes $(1\,1\,0)$ and $(1\,\bar{1}\,0)$ (106°) [18,21]. The investigations reveal that the formation of organic crystals is stimulated by the strong molecular interaction among C8-BTBT molecules with the assistance of PMMA spreading on the surface of the patterned regions [22]. Besides, anisole used in this work was a high-boiling-point (154 °C) solvent that enabled slow solvent evaporation during the spin-coating process, resulting in a thermodynamically preferred crystalline structure.

The transfer and output curves of a typical C8-BTBT crystal FET fabricated on paper substrate are presented in Fig. 4a and b, respectively. Both curves exhibited negligible hysteresis, and the gate leakage current was in the region of $10^{-15}$ A to $10^{-13}$ A. The device yielded a high performance with a $\mu_{FET}$ of 1.3 $cm^2/V\,s$ and an on/off ratio of more than $10^8$. Threshold voltage ($V_{th}$) and subthreshold swing ($S$) are −2.6 V and 2.0 V/dec, respectively. Apart from the on-current improved by the high $\mu_{FET}$, the large on/off ratio can also be attributed to the suppression of the off-current ($10^{-13}$ A). The average value of $\mu_{FET}$ for 20 devices on the same paper substrate was 0.9 $cm^2/V\,s$ with a standard deviation of 0.3 $cm^2/V\,s$. To the best of our knowledge, the current FET arrays with organic crystals possess the highest device performance in terms of both carrier mobility and on/off ratio for OFETs on paper substrates. Such significantly improved electrical performance is even comparable with that of amorphous silicon transistors, implying the potentials of the FET arrays for practical application. Additionally, the device performance was dependent with the spin-coating conditions, such as spin-coating speed and material concentration (see Supplementary content). Enhanced performance can be expected as the experimental parameters are further optimized.

Large surface roughness is a major obstacle for fabricating electronic devices on paper substrates [1]. Fig. 1d shows the atomic force microscopy (AFM) image of the

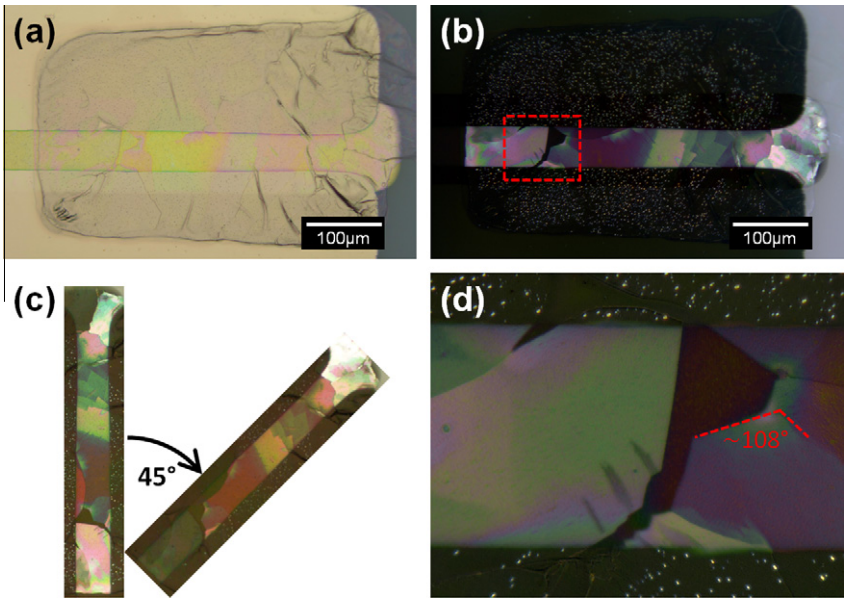


**Fig. 3.** (a) and (b) Bright-field and cross-polarized microscope images of the C8-BTBT crystals in the patterned region via a spin-coating process from the mixture solution of C8-BTBT (0.4 wt.%) and polymethylmethacrylate (PMMA; 0.1 wt.%), respectively. (c) Cross-polarized microscope images of the organic crystals in the channel region with the substrate rotated by 45°. (d) Cross-polarized microscope image of the organic crystals within the red-dotted square in the channel region of (b). The angle of facets at the crystal front end is ~108°. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

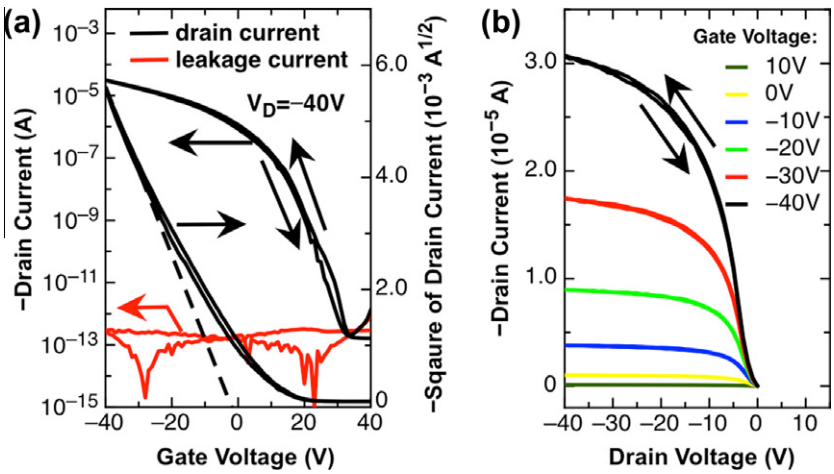


**Fig. 4.** (a) and (b) Transfer and output curves of a typical organic crystal FET on the paper substrate, respectively. The leakage current was as low as $10^{-15}$ A to $10^{-13}$ A.

surface of bare photo papers. As expected, the surface shows poor smoothness with a root-mean-square (rms) roughness of 48 nm. For the next processed layers, the rms roughness values measured from the AFM images of the surfaces of parylene, Au bottom gate, and patterned CYTOP (Fig. 1e–g) were 16, 12, and 12 nm, respectively. Although the surface roughness decreased from the bare paper substrate to the patterned CYTOP layer (Fig. 1c), it was still too large to allow for a high device performance. Poor surface characteristic of substrates can frequently result in inferior dielectric properties of the gate dielectric layer and in considerably degraded device performance because of more disordered molecular structure of the organic semiconductor on the gate dielectric [23]. Therefore, to achieve high performance, the improvement of surface characteristics should be carefully considered.

As abovementioned, spin-coating from a C8-BTBT/PMMA mixture solution leads to a double-layer structure owing to phase separation [18,19]. To elucidate the origin of the high device performance obtained from the current

FET arrays on the paper substrate, the C8-BTBT/PMMA interface was investigated by AFM studies. Considering that cyclohexane is a good solvent for C8-BTBT and cannot dissolve PMMA, the sample was rinsed in cyclohexane to remove the C8-BTBT layer. AFM characterizations on this surface showed that most of the PMMA surface was exposed after rinsing (Fig. 1h). Although partially covered with the remaining C8-BTBT, the PMMA layer had a very smooth surface with a rms roughness of 3 nm (Fig. 1c). Some patches with sizes of hundreds of nanometers were also observed. As shown in Fig. 1i, these patches had similar thicknesses (~3.8 nm). More importantly, this thickness was consistent with the length of the C8-BTBT molecule (3.3 nm) [16]. Therefore, the patches were the monolayers of C8-BTBT molecules, which acted as the first layer of C8-BTBT crystals on the PMMA layer. Such C8-BTBT monolayers observed from the AFM images indicated that the spin-coating process can produce a C8-BTBT/PMMA interface with a high-quality morphology. Furthermore, the maximum trap density ($N_{trap}$) at the C8-BTBT/PMMA interface estimated from the subthreshold swing $S$ was $7.6 \times 10^{11}$ cm$^{-2}$ [24,25]. Therefore, although fixed interface charges could be introduced during the $O_2$-plasma treatment [26], the PMMA modification from the phase-separation-introduced C8-BTBT/PMMA double layer can reduce the interfacial trap density. Such a smooth interface with low trap density also contributed to the high on/off ratio obtained in the current devices. Consequently, despite the large roughness of the paper substrates, the proposed solution-based approach can create a high-quality semiconductor/dielectric interface. Such an interface is beneficial for microscopic charge transport, and consequently, for the device performance.

## 4. Conclusion

In conclusion, solution-processed organic crystals for FET arrays on paper substrate were demonstrated. The surface wettability of the paper substrate was patterned using a highly hydrophobic dielectric. A spin-coating process under ambient conditions from a C8-BTBT/PMMA mixture solution can produce C8-BTBT crystals with grain sizes of hundreds of micrometers and a smooth C8-BTBT/PMMA interface. The FET arrays showed high device performance with a $\mu_{FET}$ reaching 1.3 cm$^2$/V s and an on/off ratio of $10^8$. These results provide a fast and low-cost manufacturing process for paper electronics. Besides, both oxygen and water could permeate paper substrates and polymer layers, and the strong acceptor of $FeCl_3$ used in source-drain electrodes could be degraded under air. An appropriate encapsulation process would benefit the air-stability against degradation in device performance. In addition, the presented method has no critical requirement for the surface smoothness of substrates. Thus, it is also promising for devices on other substrates, such as plastic ones.

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## Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at doi:10.1016/j.orgel.2012.01.021.

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